

# SP8660

## 150MHz ÷ 10

The SP8660 is a low power ECL counter with an open collector output capable of driving TTL or CMOS. It has internally biased inputs.

### FEATURES

- AC Coupled Inputs
- Low Power Consumption
- CMOS/TTL Compatible Open Collector Output

### QUICK REFERENCE DATA

- Supply Voltage: 5.0V
- Power Consumption: 50mW
- Temperature Range: -30°C to +70°C
- 8-Lead Plastic Package

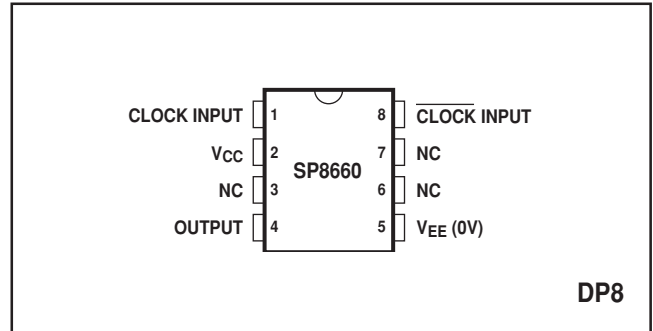


Fig. 1 Pin connections - top view

### ABSOLUTE MAXIMUM RATINGS

Supply voltage	8V
Open collector output voltage	12V
Storage temperature range	-55°C to +150°C
Max. junction temperature	+150°C
Max. clock input voltage	2.5V p-p
Output sink current	10mA

### ORDERING INFORMATION

SP8660 DP

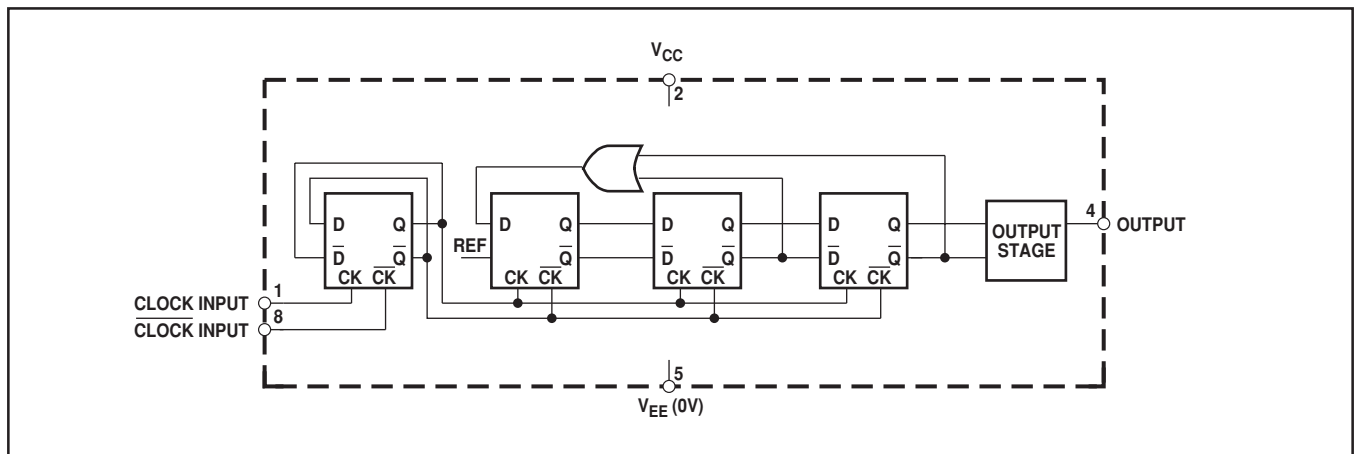


Fig. 2 Functional diagram

**ELECTRICAL CHARACTERISTICS**

Unless otherwise stated, the Electrical Characteristics are guaranteed over specified supply, frequency and temperature range

Supply voltage,  $V_{CC} = 5.0V \pm 0.25V$ ,  $V_{EE} = 0V$

Temperature,  $T_{AMB} = -30^{\circ}C$  to  $+70^{\circ}C$

Characteristic	Symbol	Value		Units	Conditions
		Min.	Max.		
Maximum frequency (sinewave input)	$f_{MAX}$	150		MHz	Input = 200-1000mV p-p
Minimum frequency (sinewave input)	$f_{MIN}$		40	MHz	Input = 400-1000mV p-p
Power supply current	$I_{CC}$		13	mA	$V_{CC} = 5.25V$
Output high voltage	$V_{OH}$	9		V	$V_{CC} = 5V$ , pin 4 = $1.5k\Omega$ to 10V, see note 3
Output low voltage	$V_{OL}$		400	mV	$V_{CC} = 5V$ , pin 4 = $1.5k\Omega$ to 10V, see note 3

**NOTES**

1. The test configuration for dynamic testing is shown in Fig.5.
2. All characteristics above are tested at  $25^{\circ}C$  only.
3.  $C_{LOAD} \approx 5pF$ .

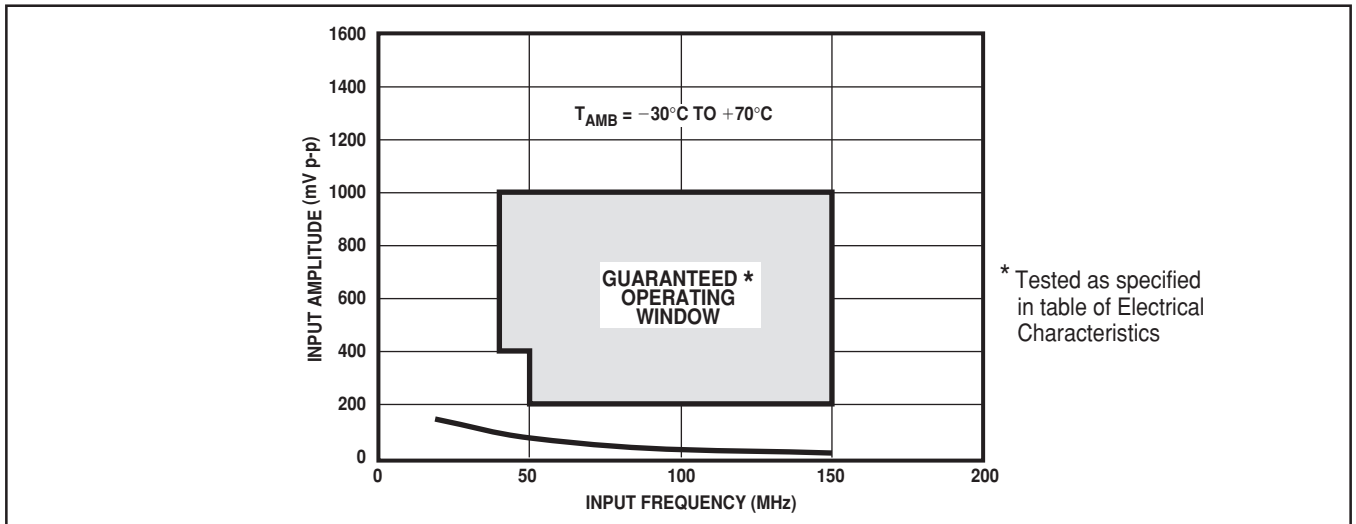


Fig. 3 Typical input characteristic

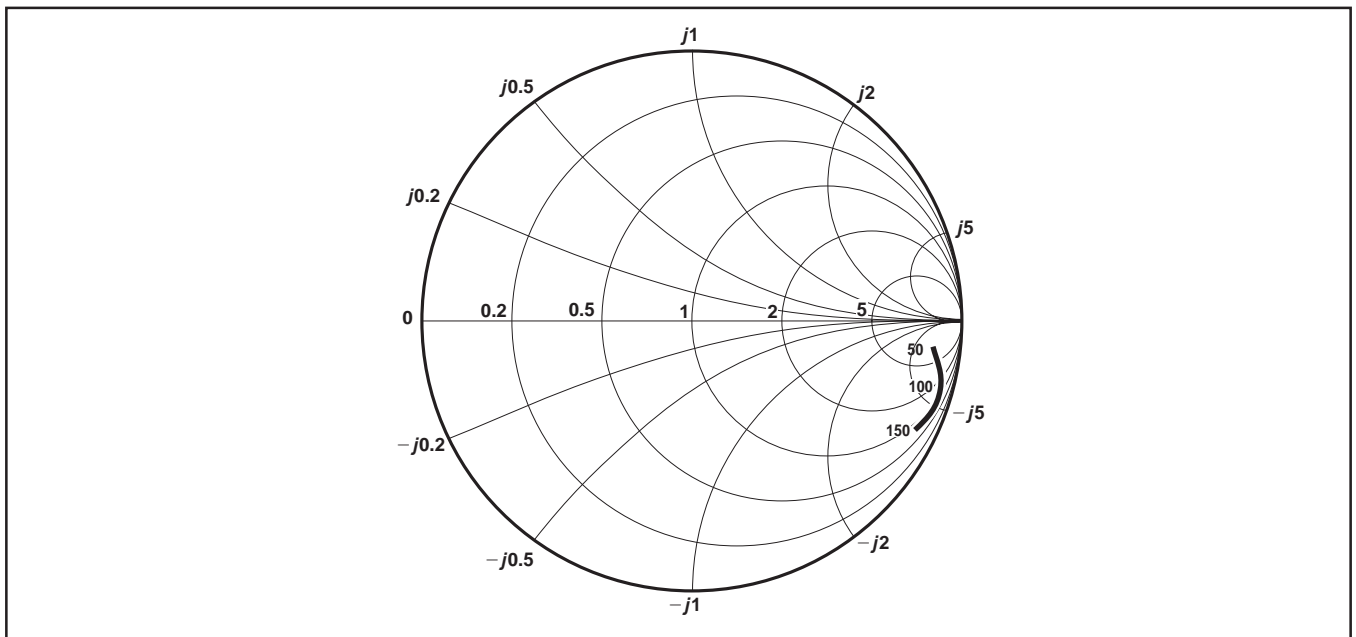


Fig. 4 Typical input impedance. Test conditions: supply voltage =  $5.0V$ , ambient temperature =  $25^{\circ}C$ , frequencies in MHz, Impedances normalised to  $50\Omega$

**OPERATING NOTES**

1. The clock inputs (pins 1 and 8) should be capacitively coupled to the signal source. When driven single ended, the input signal path is completed by a capacitor from the unused input to ground.
2. In the absence of a signal the devices will self-oscillate. This can be prevented by connecting a 39kΩ resistor from either input to ground. If the device is driven single ended, it is recommended that the pull-down resistor be connected to the decoupled unused input. There will be a loss in sensitivity of approximately 200mV.
3. The device will operate down to DC but input slew rate must be better than 100V/μs.
4. The open collector output will drive three TTL loads, and therefore requires a a suitable resistor to V<sub>CC</sub> to maintain noise immunity. In order to maintain noise immunity on transitions, this

resistor should not exceed 4-7kΩ. For interfacing to CMOS, the open collector may be restored to a +10V line via a 3.3kΩ resistor. The output sink current must not exceed 10mA and the use of too low a value of resistor may lead to a loss of noise immunity, especially at low temperatures.

5. Input impedance varies as a function of frequency; see Fig. 4.
6. The rise time of the open collector output waveform is directly proportional to the load capacitance and load resistor value. Therefore, the load capacitance should be minimised and the load resistor kept to a minimum compatible with system power requirements.

In the test configuration of Fig. 5, the output rise time is approximately 20ns and the fall time is typically 10ns.

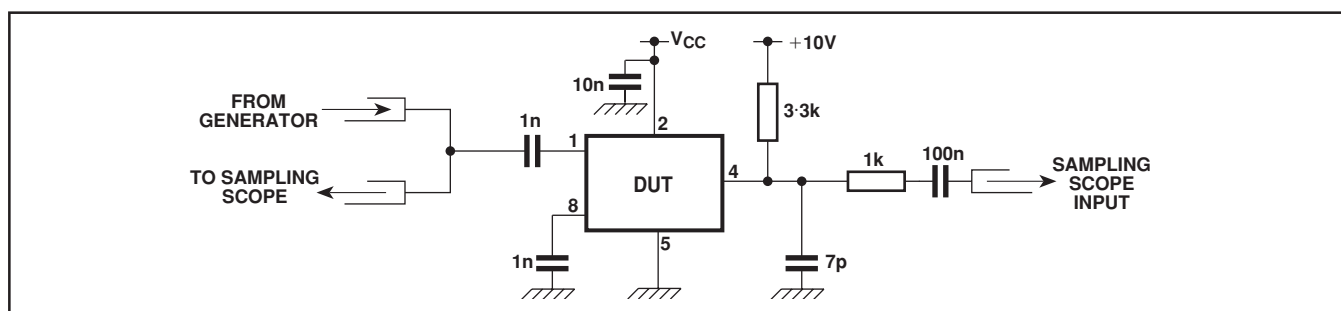


Fig. 5 Test circuit

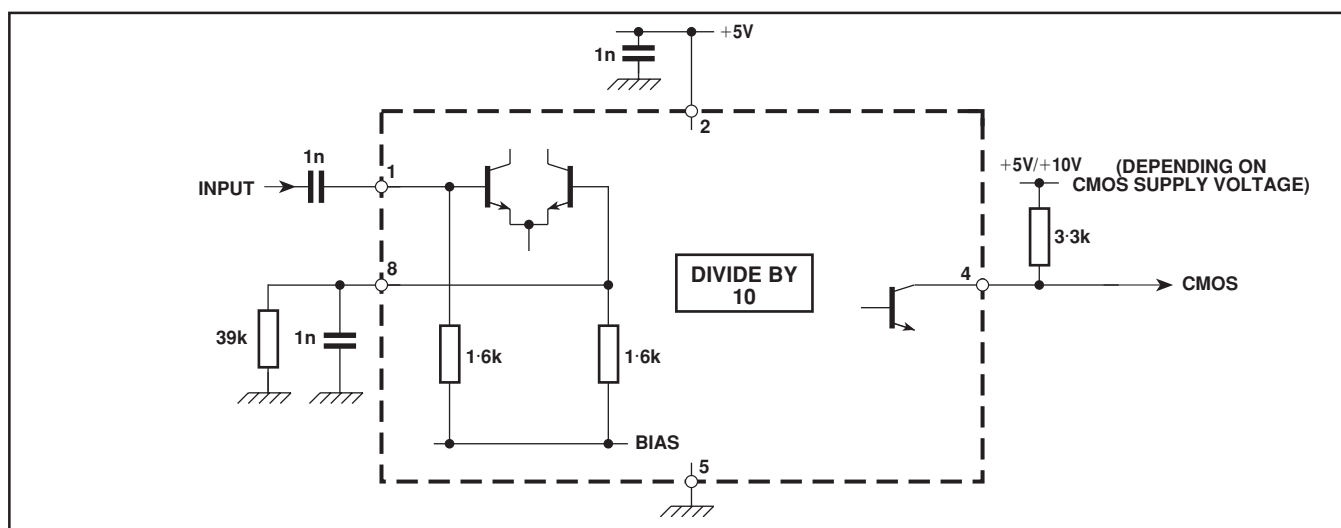


Fig. 6. Typical application circuit showing interfacing

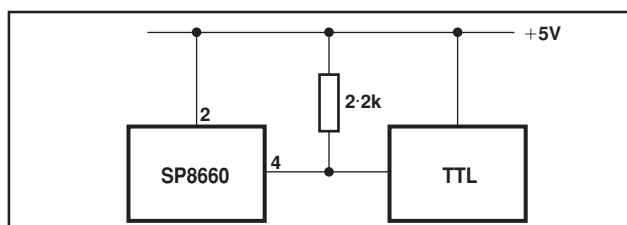
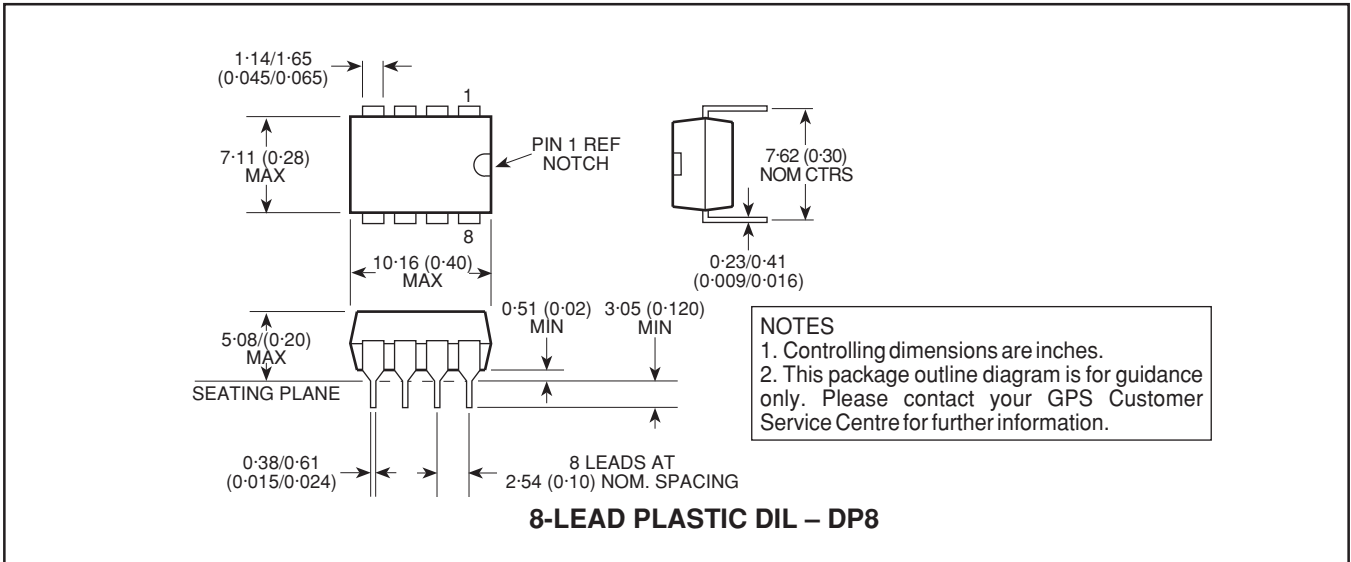


Fig. 7. Interfacing to TTL. Load not to exceed 3 TTL unit loads

**PACKAGE DETAILS**

Dimensions are shown thus: mm (in).



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